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Circuit Card Layout Considerations for 10Gbps Current Mode Logic Inputs on the MAX3950 EV Kit

MAXIM High-Frequency/Fiber Communications Group

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1 Introduction

Interfacing 10Gbps current mode logic (CML) signals using controlled-impedance microstrip signal paths on circuit cards requires appropriate material selection and careful attention to layout geometry in order to control crosstalk and signal integrity. The following example from the MAX3950 10Gbps 1:16 deserializer evaluation kit (EV kit) board illustrates some key points.

The MAX3950 EV kit was constructed to provide a means for characterization and testing of the MAX3950 10Gbps 1:16 deserializer with 10Gbps differential CML clock and data inputs, and 16 622Mbps LVDS outputs. Four edge-mount SMA connectors carry the differential 10Gbps clock and data inputs, and 32 SMB connectors spaced symmetrically around the MAX3950 carry the delay-matched 622Mbps deserialized data outputs.

2 Microstrip Design

The outer layers of the evaluation board were constructed from Rogers Corporation RO4350® microwave laminate, which was selected because it is cost-effective, has a low dielectric constant, and is compatible with conventional FR-4 fabrication methods. The MAX3950 IC is packaged in a 68-lead QFN package with 20mil lead pitch. The artwork for the first two component-side layers, which carry the microstrip transmission lines, is reproduced in Figures 1 and 2. Note the test structures for evaluation of transmission-line characteristics on the right-hand board edges.

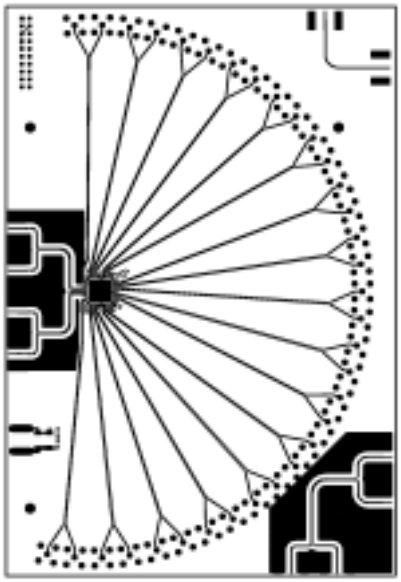

Figure 1. EV kit PC-board layout (top-layer component side)

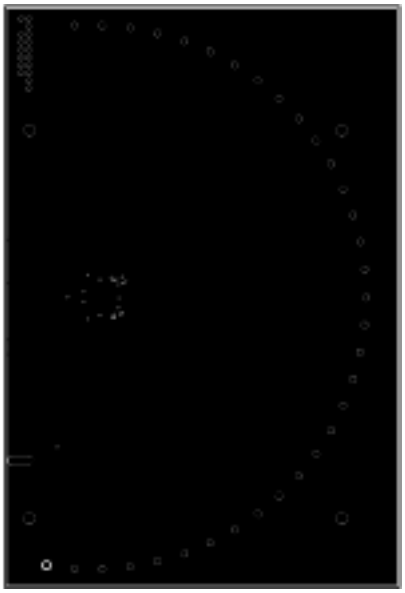

Figure 2. EV kit PC-board layout (ground plane)

Because the MAX3950 10Gbps CML clock and data inputs are differential signals, a coupled-microstrip design was used for each signal input, with characteristic impedance of Z_{diff} = 100Ω. Compared to single-ended microstrip lines, coupled-microstrip transmission lines yield better delay matching and reduced sensitivity to board-thickness variations for long trace lengths. Coupled-microstrip lines are also more compact, providing geometries that easily interface with the QFN package.

An Excel spreadsheet was employed to compute initial values for the conductor size and spacing, using the equations of Gupta, et al. (see References), then Sonnet Lite® was used to validate the design.

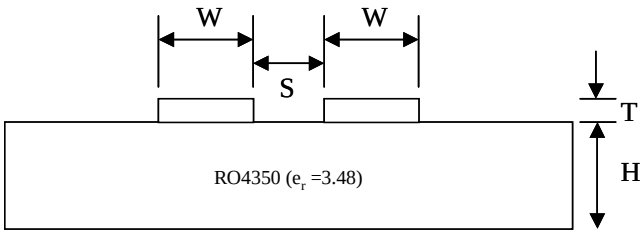

Figure 3. Coupled-microstrip geometry (side view)

The geometry of the coupled-microstrip is shown in Figure 3, and the dimensions for both the single-ended and the differential microstrip structures used on the EV kit board are given in Table 1.

Table 1. Microstrip Dimensions

Rogers RO4350 (ε_r = 3.48)	**Height (H)**	**Width (W)**	**Separation (S)**	**Thickness (T)**
Single-Ended (near connectors)	10 mil	22 mil	NA	0.35 mil
Differential (50Ω coupled microstrip)	10 mil	12.5 mil	10 mil	0.35 mil
Differential (near IC pads)	10 mil	10 mil	10 mil	0.35 mil

Figure 4 shows an enlarged view of one 10Gbps CML input signal path on the top conductor layer (built on Rogers RO4350® laminate) of the printed circuit card. Note that there are three distinct configurations (regions) of the microstrip transmission line. On the far left of the EV kit board, the positive and negative CML inputs transition from a pair of edge-mount SMA connectors into two independent (single-ended) 50Ω microstrip transmission lines, each with 22mil line width. Two 0402-size AC-coupling capacitors (0.01µF) are incorporated into the dual microstrip transmission lines, which then transition into a coupled-microstrip (differential) transmission line, with 12.5mil line width and 10mil separation (just before the second bend). Finally, there is a transition region of about 200mil length near the IC (after the final bend) where the coupled-microstrip trace width and conductor spacing are both 10mil, which matches the lead width and spacing on the QFN package.

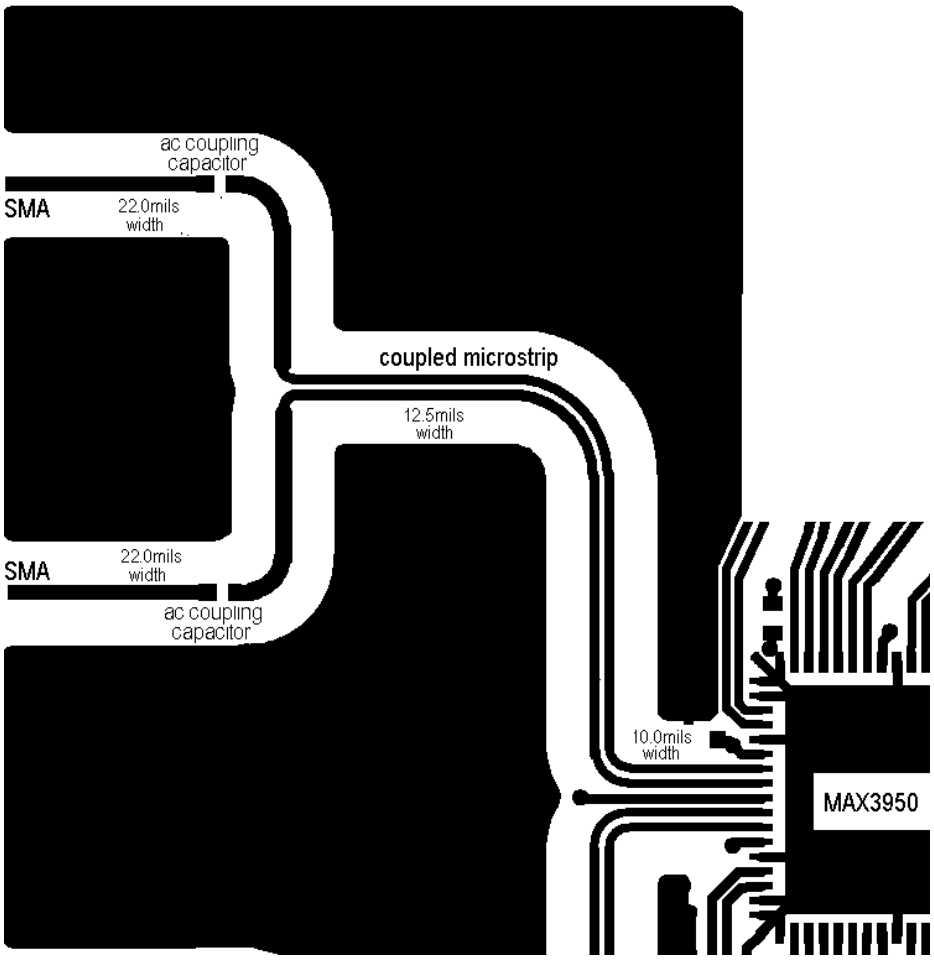

Figure 4. 10Gbps microstrips near the IC package

3 Results

When the MAX3950 EV kit board was examined on a differential network analyzer, the minimum return loss for the signal path from the board input (excluding the SMA connector) into the MAX3950 deserializer IC was 15dB between 0 and 15GHz. These results were very close to the simulation data shown in Figure 5, which includes the MAX3950 package and input termination structure.

It is particularly important, when routing long interconnections at 10Gbps, to use an impedance-matched microstrip transmission line structure. For differential CML, the coupled-microstrip transmission line, described in Table 1, provides both good geometric match with the lead spacing on the QFN package and good electrical match into the input of the MAX3950 IC.

In summary, the MAX3950 EV kit board demonstrates the use of coupled-microstrip transmission lines for differential 10Gbps CML signals, with a high-performance microwave-laminate material for the microstrip dielectric layer. It would be prudent to confirm the performance of your own specific transmission-line geometry through both simulation and measurement. For assistance in circuit-card layout using Maxim's 10Gbps fiber optic products, contact your Maxim Integrated Products fiber applications engineer.

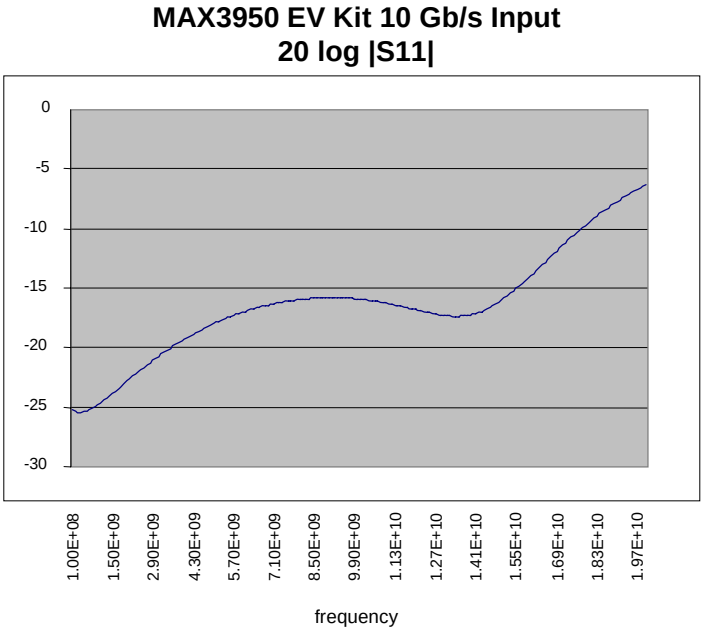

Figure 5. MAX3950 input signal path |S11| simulation, not including SMA connectors

References

Collin, Robert E., *Foundations for Microwave Engineering*, McGraw-Hill, 2d Ed., 1996, page 165.

Gupta, et al., *Microstrip Lines and Slotlines*, Artech House, 1979